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Harmonic Mitigation in Various Levels of Multilevel Inverter with Different Loads

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Abstract - Cascade Multilevel Inverters are very popular and have many applications in electric utilities and for industrial drives. When these inverters are used for industrial drives directly, the THD in the output voltage of inverters is very significant as the performance of drive depends very much on the quality of voltage applied to drive. A multilevel inverter in high power ratings improves the performance of the system by reducing harmonics. This paper presents the simulation of single phase nine level, eleven level and thirteen level inverters. Detailed analysis of these inverters has been carried out and compared with different loads. PWM control strategy is applied to the switches at appropriate conducting angles with suitable delays. These different level inverters are realized by cascade H-Bridge in MATLAB/SIMULINK. The inverters with a large number of steps can generate high quality voltage waveforms. The THD depends on the switching angles for different units of multilevel inverters. It has been found that the fifteen level CMLI satisfies this limit while seven and eleven level CMLI do not meet this limit.

Keywords: Cascaded H-bridge inverter, PWM, THD.

I. INTRODUCTION

Multilevel inverters (MLI) are becoming popular than two level inverter in high power applications. Multilevel output is synthesized by small dc voltage levels. In multilevel inverters all the switches are connected in series which allows operation at higher voltage level [1]. The main advantages of MLI are high voltage capability, low switching losses, low dv/dt , less THD, less electromagnetic compatibility [1-2]. The main three MLI configurations are neutral point converter, flying capacitor and cascaded H-bridge multilevel inverter [3]. CHMI has more advantages than other two mentioned. CHMI does not have flying capacitors and clamping diodes. Main drawback of CHMI is that the number of devices used increases with the number of levels [4] and this increases the gate drive circuits at control stage itself causing high cost and switching losses [5]. To overcome above disadvantages the choice is hybrid multilevel inverter which is derived from cascaded H-bridge inverter. In order to control the MLI output voltage there are several control techniques in the literature. The most efficient methods are based on sinusoidal PWM techniques because it leads to easy control of inverter's fundamental voltage and as well as eliminates the harmonics. Among various PWM techniques, phase disposition sinusoidal pulse width modulation (PDSPWM) technique is most popular because of its simplicity to apply in CHMI and HMI control with increase in number of levels

Harmonic content decreases as the number of levels increases thus reducing the filtering requirements. Without an increase in the rating of an individual device, the output voltage and power can be increased. The switching devices do not encounter any voltage sharing problems. The simulation of single phase nine level, eleven level and thirteen level inverters is done in MATLAB (Simulink). The FFT spectrums for the outputs are compared and presented to validate the proposed control strategy.

II. MULTILEVEL INVERTERS

The voltage source inverters produce an output voltage or a current with levels either $0,+V_{dc}$, $-V_{dc}$. They are known as the two-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various pulse width modulation strategies. The multilevel inverters have drawn tremendous interest in the power industry. It may produce high-power, high-voltage inverter with the multilevel structure because of the device, which voltage stresses are controlled in the structure.

- Have less switching device as far as possible.
- Be capable of withstanding very high input voltage.
- Have lower switching frequency for each switching devices.

Multilevel inverters generate a staircase waveform. By increasing the number of output levels, the output voltages have more steps and harmonic content on the output voltage and the THD values are reduced. Therefore, they produce high quality output voltage by increasing the number of levels. Different topologies available in multilevel inverters are as follows.

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- Diode Clamped Multilevel Inverter
- Capacitor Clamped Multilevel Inverter
- Cascaded H-Bridge Multilevel Inverter

In Cascaded H-bridge multilevel inverter topology, the H-bridges are cascaded in every phase. With the increase in H-bridges in a phase, the output voltage waveform is tends to be more sinusoidal. In n- level topology, (n-1)/2 identical H-bridges are used in every phase. There must be a separate DC source for the DC bus of every individual H-bridge. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, $-V_{dc}$ (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from $-V_{dc}$ to $+V_{dc}$ with three levels, $-2V_{dc}$ to $+2V_{dc}$ with five-level and $-3V_{dc}$ to $+3V_{dc}$ with seven-level inverter. x The number of output phase voltage levels in a cascaded inverter is defined by

$$m=2s+1. \quad .. \quad (1)$$

where, s - is the number of dc sources.

The cascade multilevel inverter consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series as shown in Fig.1 Each H-bridge can produce three different voltage levels: +Vdc, 0 and –Vdc by connecting the dc source to ac output side by different combinations of the four switches S1, S2, S3, and S4. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs. By connecting sufficient number of H-bridges in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized.

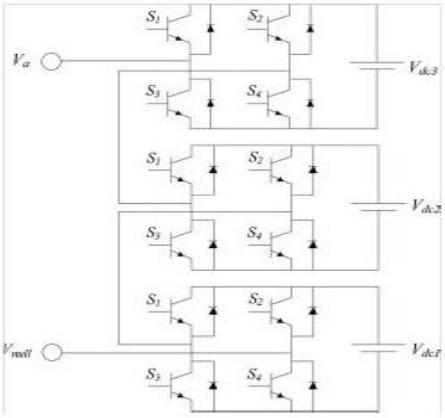

Figure 1 Topology of Cascaded Multilevel Inverter

The number of levels in the output phase voltage and line voltage are 2*s*+1 and 4*s*+1 respectively, where *s* is the number of H-bridges used per phase. For example, Three H- Bridges, Five H-bridges and Seven H-bridges per phase are required for 7-level, 11-level and 15-level multilevel inverter respectively. The magnitude of the ac output phase voltage is the sum of the voltages produced by H-bridges.

Table 1 Comparison between Different Level Inverter Topologies

S.No	Topology	Diode Clamped	Flying Capacitor	Cascaded H-Bridge
1.	Power semi conductor Switches	2(m-1)	2(m-1)	2(m-1)
2.	Clamping diodes per phase	(m-1) (m-2)	0	0
3.	DC bus capacitors	(m-1)	(m-1)	(m-1)/2
4.	Balancing capacitors per phase	0	(m-1) (m-2)/2	0
5.	Voltage un balancing	Average	High	very small

III. METHODS FOR HARMONIC REDUCTION IN INVERTERS

One of the most important aspects of a system is the reduction of harmonics that are present in the system. In case of an inverter, it is very important to remove the harmonics from the ac output. The harmonics present in a dc to ac inverter are very much obvious compared to the harmonics that can be present in an ac to dc converter. This is because of the output of dc to ac inverter being ac. Thus, the filters that are used in dc to ac inverter have different designs compared to the filters used in ac to dc converters. In case of ac to dc converters, the main objective is to improve the output voltage ripple. Thus, passive filters can be easily used in order to improve the output of an ac to dc converter. While, in case of dc to ac inverter, the harmonic reduction is harder and it also includes the use of active filters. As the output of dc to ac inverters is alternating, it is very important to produce sinusoidal output waveforms. The filters used to remove the harmonics from the inverters are more complex and consists of large number of inductors and capacitors to remove the harmonics of higher order. Thus, in order to avoid the cost of such expensive and complex filters controlling the width or reducing the number of pulses may result into reduction of harmonics. One such technique is explained below.

IV .SELECTIVE HARMONIC ELIMINATION

Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) technique is one of the control techniques for inverters. It is mainly used for reducing the harmonic content in single phase and three phase inverters and

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to improve the power quality. The selection of switching angles for eliminating particular harmonic is difficult. The elimination of low-order harmonics is an important issue in power electronics applications. Selective Harmonic Elimination (SHE) is a low switching frequency strategy that uses calculated switching angles to eliminate certain harmonics in the output voltage. With the help of Fourier series analysis the amplitude of any odd harmonic in the output signal can be calculated. The switching angles must however be lower than $\frac{\pi}{2}$ degree and for a number of switching angles a harmonic component can be affected, where number of harmonics can be eliminated. If angles were to be larger than $\frac{\pi}{2}$ correct output signal would not be achievable. Higher harmonics can be filtered out with additional filters added between the inverter and the load if needed. Performance of inverter is improved by incorporating selective harmonic elimination. In this method the switching angles are computed such that a desired fundamental sinusoidal voltage is produced while at the same time certain order harmonics are eliminated.

Lower Order Harmonic: The LOH is that harmonic component whose frequency is closest to the fundamental one, and its amplitude is greater than or equal to 3% of the fundamental component.

Higher Order Harmonic: The HOH is that harmonic component whose frequency is far away from the fundamental one.

Other Order Harmonic: Even order harmonics is a one which is the multiple of two. For example, second-order harmonic is two times the frequency of the fundamental, and a fourth-order harmonic is four times the frequency of the fundamental and so on. Odd order harmonics includes third, fifth, seventh, eleventh and so on. The triple harmonics are those which are the multiples of fundamental one with three. E.g., third, ninth and so on are third order harmonics, which gets cancelled out in three phase applications.The Fourier series expansion of a periodic signal is given by:

$$f(t) = a_v + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_\circ t) + b_n \sin(2\pi n f_\circ t)$$

$$\text{where, } a_v = \frac{1}{T}\int_{t_\circ}^{t_\circ+T} f(t)dt,$$

$$a_n = \frac{2}{T}\int_{t_\circ}^{t_\circ+T} f(t)\cos(2\pi n f_\circ t)dt,$$

$$b_n = \frac{2}{T}\int_{t_\circ}^{t_\circ+T} f(t)\sin(2\pi n f_\circ t)dt$$

For a signal with Odd-Quarter wave symmetry,

$a_v = 0$,

$a_n = 0$; for all n,

$b_n = 0$; for n even, and

$$b_n = \frac{8}{T}\int_0^{T/4} f(t)\sin(2\pi n f_\circ t)dt \quad \text{for n odd}$$

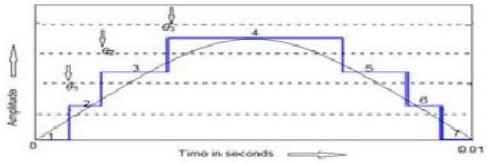

Figure 2 Output phase voltage waveform for 7-level CMLI

The wave that exhibits odd quarter wave symmetry is,

$$b_n = \frac{4}{\pi n} V_{dc}\left[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)\right]$$

The Fourier output voltage equation of multilevel inverter with three separate DC sources.

$$V_n(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t)$$

Where, V_n is the amplitude of the n-th harmonic.

Because of odd quarter-wave symmetric characteristic, harmonics with even order become zero. Consequently, V_n becomes,

$$V_n = \begin{cases} \frac{4V_{dc}}{n\pi}\sum_{i=1}^{s}\cos(n\theta_i) \\ 0 \end{cases}$$

So, to satisfy fundamental harmonic and to eliminate the fifth and seventh harmonics, three nonlinear equations with three angles are provided in

$$V_1 = \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3)]$$

$$V_5 = \frac{4V_{dc}}{5\pi}[\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3)]$$

$$V_7 = \frac{4V_{dc}}{7\pi}\left[\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3)\right] \quad (2)$$

It is shown that, V_5 and V_7 are set to zero in order to eliminate fifth and seventh harmonics, respectively. For obtaining various switching angles a new index, titled modulation index, is defined to be a representative of V1:

$$M = \frac{V_1}{12V_{dc}/\pi} \quad (0 \le M \le 1)$$

Here, M is chosen between 0 and 1 to cover different values of V_1. Now, three switching angles, namely θ_1, θ_2, and θ_3 must be found with respect to the range of M.

In general, the Fourier series expansion of the staircase output voltage wave form as shown in Fig.2 is given by,

$$V_{an}(wt) = \alpha,\ k=1,3,5...$$

where,

s is the number of H-bridges connected in cascade per phase

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and *k* is order of harmonic components.

For a given desired fundamental peak voltage *V1*, it is required to determine the switching angles such that $0 \leq \alpha_1 < \alpha_2 \ldots < \alpha_S \leq \pi/2$ and some predominant lower order harmonics of phase voltage are zero. Among *S* number of switching angles, generally one switching angle issued for fundamental voltage selection and the remaining(*s*-1) switching angles are used to eliminate certain predominating lower order harmonics. In three-phase power system, triplen harmonic components are absent in line-to-line voltage, as a result, only non-triplen odd harmonic components are present in line-to-line voltages [4-5]. From equation (3) the expression for the fundamental voltage in terms of switching angles is given by,

$$4V_{dc} = [\cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_3)] = V_1 \quad (1)$$

(3)

Moreover, the relation between the fundamental voltage and the maximum obtainable voltage is given by modulation index. The modulation index, *m*, is defined as the ratio of the fundamental output voltage (*V1*) to the maximum obtainable fundamental voltage. The maximum fundamental voltage is obtained when all the switching angles are zero .i.e.

V1max=4sVdc/π, therefore, $m = \pi V1/4sVdc$ (4)

For 7, 11 and 15-level cascade multilevel inverters, *s*=3,*s*=5 and *s*=7 respectively. Number of degrees of freedom available is equal to *s* one degree of freedom is used to choose the value of *V1*and the remaining degrees of freedom are used to eliminate the lower order harmonic components. In case of 7-level CMLI, only two harmonic components (in general,5th and 7th) can be eliminated, similarly for 11-level CMLI, four harmonic components (i.e.5th, 7th, 11th and 13th) and in 15-level CML1 six harmonic components (i.e. 5th, 7th, 11th, 13th, 17th and 19th) can be eliminated.

From equation (5), the expressions for fundamental voltage in terms of *m*, and lower order harmonic components, when they are eliminated, can be written as for 7-level CMLI:

$\cos(\alpha1)+\cos(\alpha2)+\cos(\alpha3) = 3m$
$\cos(5\alpha1)+\cos(5\alpha2)+\cos(5\alpha3)=0$
$\cos(7\alpha1)+\cos(7\alpha2)+\cos(7\alpha3)=0$ (5)

For 9-level CMLI, corresponding equations are as follows:

$\cos(\alpha1)+\cos(\alpha2)+\cos(\alpha3)= 4m$
$\cos(5\alpha1)+\cos(5\alpha2)+\cos(5\alpha3)=0$
$\cos(7\alpha1)+\cos(7\alpha2)+\cos(7\alpha3)=0$
$\cos(11\alpha1)+\cos(11\alpha2)+\cos(11\alpha3)=0$ (6)

For 11-level CMLI, corresponding equations are as follows:

$\cos(\alpha1)+\cos(\alpha2)+\cos(\alpha3)= 5m$
$\cos(5\alpha1)+\cos(5\alpha2)+\cos(5\alpha3)=0$
$\cos(7\alpha1)+\cos(7\alpha2)+\cos(7\alpha3)=0$
$\cos(11\alpha1)+\cos(11\alpha2)+\cos(11\alpha3)=0$
$\cos(13\alpha1)+\cos(13\alpha2)+\cos(13\alpha3)=0$ (7)

For 13-level CMLI, corresponding equations are as follows:

$\cos(\alpha1)+\cos(\alpha2)+\cos(\alpha3)=6m$
$\cos(5\alpha1)+\cos(5\alpha2)+\cos(5\alpha3)=0$
$\cos(7\alpha1)+\cos(7\alpha2)+\cos(7\alpha3)=0$
$\cos(11\alpha1)+\cos(11\alpha2)+\cos(11\alpha3)=0$
$\cos(13\alpha1)+\cos(13\alpha2)+\cos(13\alpha3)=0$
$\cos(17\alpha1)+\cos(17\alpha2)+\cos(17\alpha3)=0$ (8)

For 15-level CMLI, corresponding equations are as follows:

$\cos(\alpha1)+\cos(\alpha2)+\cos(\alpha3)=7m$
$\cos(5\alpha1)+\cos(5\alpha2)+\cos(5\alpha3)=0$
$\cos(7\alpha1)+\cos(7\alpha2)+\cos(7\alpha3)=0$
$\cos(11\alpha1)+\cos(11\alpha2)+\cos(11\alpha3)=0$
$\cos(13\alpha1)+\cos(13\alpha2)+\cos(13\alpha3)=0$
$\cos(17\alpha1)+\cos(17\alpha2)+\cos(17\alpha3)=0$
$\cos(19\alpha1)+\cos(19\alpha2)+\cos(19\alpha3)=0$ (9)

The equations (4-9) are transcendental equations, known as selective harmonic elimination (SHE) equations, where unknown parameters are switching angles. The first equation of the set of equations given by (4-9) determines the magnitude of fundamental voltage for a given value of *m*, and the remaining equations eliminate selective harmonic components [11]. The equations are to be solved by employing N-R method in such a way that all possible solutions for a given value of m *are* obtained without much computational effort.

V.EXISTING METHOD

The Newton-Raphson (N-R) method is one of the fastest iterative methods. This method begins with an initial approximation and generally converges at a zero of a given system of nonlinear equations. The N-R method is to be implemented to compute the switching angles for the system given by (4-9). The Switching angles which are in the range of 0 to $\pi/2$ producing desired fundamental voltage along with elimination of 5th ,7th, 11th,and 13th harmonic components for a given modulation index are feasible solutions. The N-R method implemented was based on trial and error method for estimation of initial guess and for which solutions exist. Once a solution set was obtained, successive solutions were computed by using previous solution set as initial guess for the next one; proceeding in this way, only one solution set was obtained. Here, the N-R method is implemented in a different way for which an arbitrary initial guess between 0 to $\pi/2$ is assumed and switching angles (keeping all switching angles in the feasible range) along with the error (% content of 5th, 7th, 11th and 13th harmonic components) are computed for complete range of by incrementing its value in small steps (say 0.0001). The different solution sets are obtained for a particular range of where they exist i.e. the error is zero for feasible solutions; after getting preliminary solution sets, complete solution sets are computed by using known solutions as initial guess.

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VI.PROPOSED WORK

In Conventional methods equal conducting angles are chosen for multilevel inverters. In this method harmonics were found in output voltage of multilevel inverter. Then the method involves solving for harmonic equations using theory of resultants. Since the output waveform of multilevel inverter follows Fourier series different methods makes use of Fourier series for generating desired sinusoidal waveform through numerical equations. Software packages such as Mathematical and Math-cad is used for solving these harmonic equations. In Newton–Raphson (N–R) method is also used to solve the non-linear equations the disadvantage of iterative methods is their dependence on an initial guess and divergence problems are likely to occur for large numbers of inverter levels. Also, they can only find one set of solutions. In Gauss–Newton method it is complicated and time-consuming and requires new expression when voltage level or input dc voltage is changed. This method does not suggest any optimum solution; the second group of methods has been applied based on evolutionary algorithms. These methods are simple and can be used for problems with any number of levels. They are free from derivation. The algorithm is also used to solve these equations; Genetic Algorithm is widely used and is simpler and more applicable. But the probability of reaching to a global solution and the effect of running times is very slow.

Sinusoidal PWM

Sinusoidal Pulse Width Modulation is one of the most popular modulation techniques among the others applied in power switching devices. In case of sinusoidal pulse width modulation, all the pulses are modulated individually. A sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. The fundamental frequency SPWM control method was proposed to minimize the switching losses. It has more total harmonic distortion.

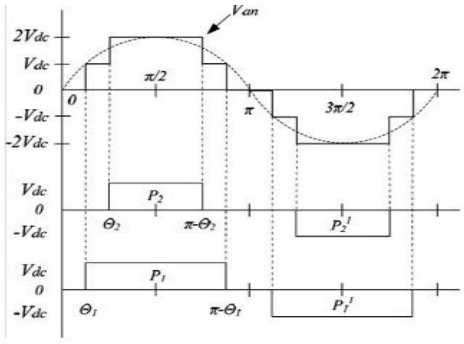

Figure 3 Sinusoidal PWM

Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals.A number of –cascaded cells in one phase with their carriers shifted by an angle and using the same control voltage produce a load voltage with the smallest distortion. The effect of this carrier phase-shifting technique can be clearly observed this result has been obtained for the multi-cell inverter in a seven-level configuration, which uses three series-connected cells in each phase. The smallest distortion is obtained when the carriers are shifted by an angle of. A very common practice in industrial applications for the multilevel inverter is the injection of a third harmonic in each cell. Another advantageous feature of multilevel SPWM is that the effective switching frequency of the load voltage is times the switching frequency of each cell, as determined by its carrier signal. This property allows a reduction in the switching frequency of each cell, thus reducing the switching losses.

BLOCK DIAGRAM

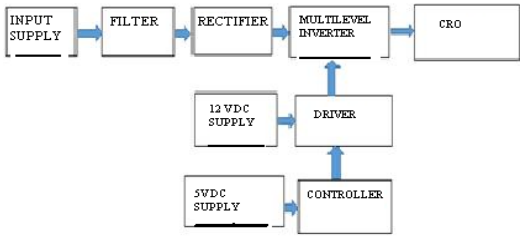

Figure 4 Block Diagram for Proposed Method

VII.RESULTS AND DISCUSSIONS

Load harmonics can cause the over heating of the motor. On the other hand source harmonics are generated by power sypply. The multilevel inverter was introduced to increase the converter output voltage as the number of level are increase the systhesis output waveform has more steps which produce stair case wave that approach the desire waveform. Hence a proposed model simulated different various levels of inverter with different loads and compare to other level.

Cascaded Multilevel Inverter (9Level)

A single phase PWM inverter consists of a PWM generator, cascaded H-bridge with dc source shown in figure 5. In this PWM generator triangular carrier wave is compared with sinusoidal modulating wave. Fig 6 shows the output voltage for 9 level CMLI. Figure 7, 8, 9 & 10 shows the different THD analysis for R,RL,RLC & motor loads.

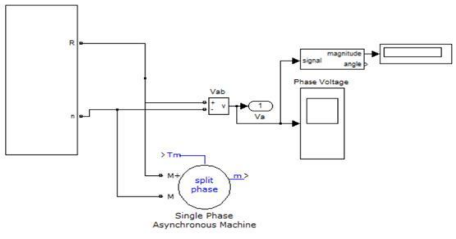

Figure 5 Simulink Diagram for 9 level CMLI

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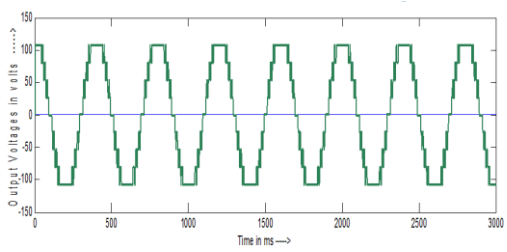

Figure 6 Output Waveform for 9 Level

FFT Analysis

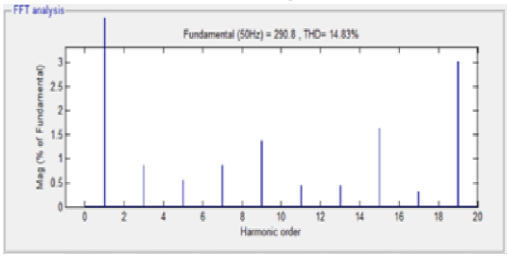

Figure 7 FFT Analysis for R-Load

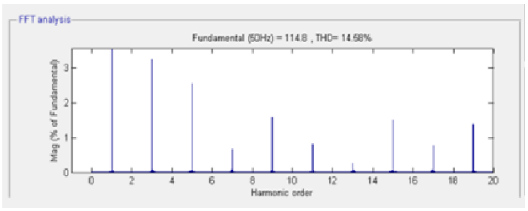

Figure 8 FFT Analysis for RL-Load

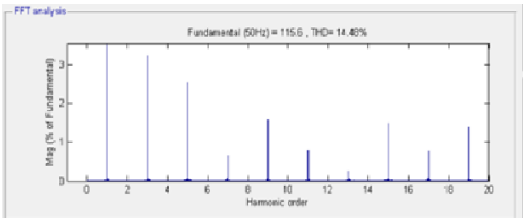

Figure 9 FFT Analysis for RLC-Load

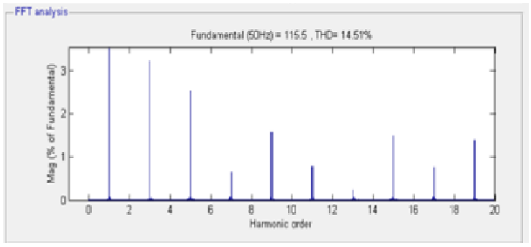

Figure 10 FFT Analysis for Motor Load

Cascaded Multilevel Inverter for 11 Level

In similar way as discussed in case of eleven -level CMLI, switching angles are calculated by using equation (7). The harmonic components of 5th, 7th, 11th and 13th orders are eliminated. Figure 12 shows the output voltage for 9 levels CMLI. Figure 13, 14, 15 & 16 shows the different THD analysis for R, RL, RLC & motor loads.

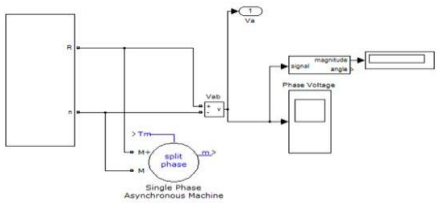

Figure 11 Simulink Diagram for 11 level CMLI

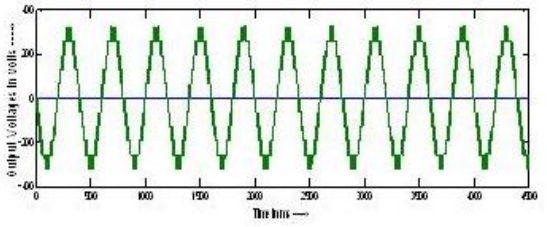

Figure 12 Output Waveform for 11 Level

FFT Analysis for 11 Level Inverter

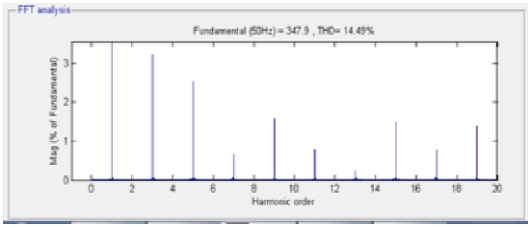

Figure 13 FFT Analysis for R-Load

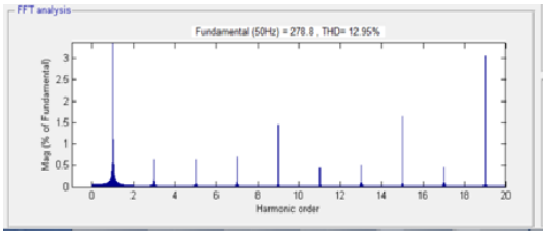

Figure 14 FFT Analysis for RL-Load

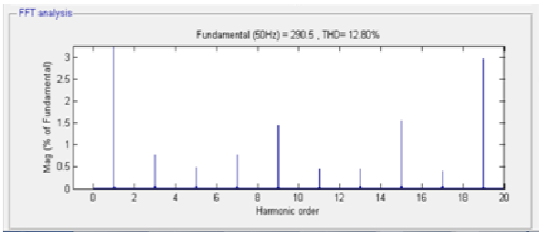

Figure 15 FFT Analysis for RLC-Load

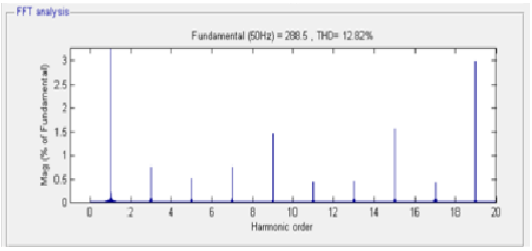

Figure 16 FFT Analysis for Motor Load

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Cascaded Multilevel Inverter for 13 Level

In this case, more number of harmonic components (six) as compared to9 and 11 level CMLIs THD contents in output voltage reduces appreciably. The harmonic components eliminated are 5th, 7th, 11th, 13th, 17th and 19th. Figure 18 shows the output voltage for 13 levels CMLI. Fig 19, 20,21 & 22 shows the different THD analysis for R,RL,RLC & motor loads.

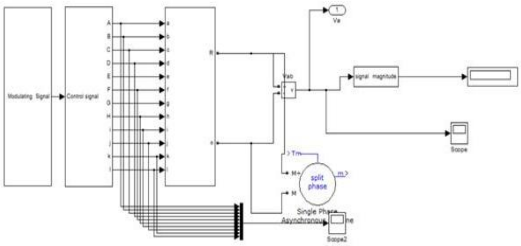


Figure 17 Simulink Diagram for 13 level CMLI

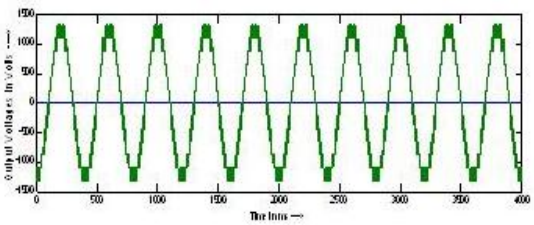


Figure 18 Output Waveform for 13 Level

FFT Analysis for 13 Level Inverter

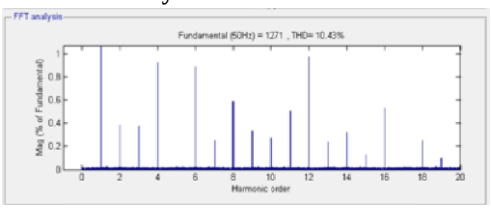


Figure 19 FFT Analysis for R-Load

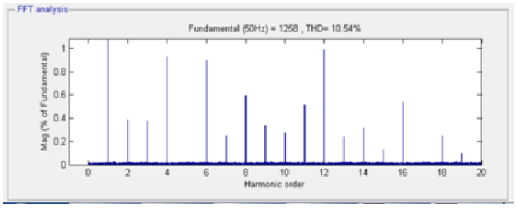


Figure 20 FFT Analysis for RL-Load

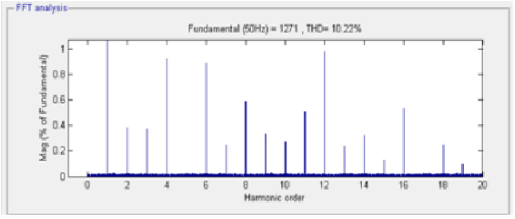


Figure 21 FFT Analysis for RLC-Load

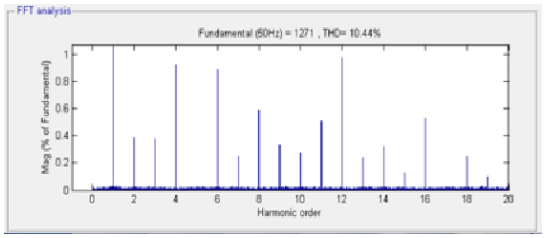
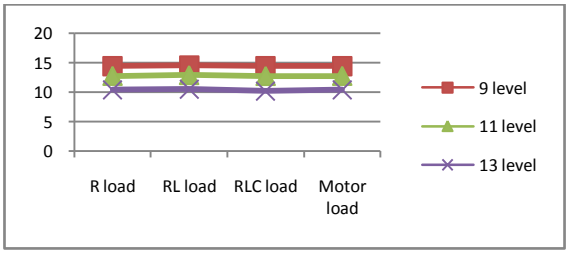


Figure 22 FFT Analysis for Motor Load

Table 2 Comparison of different Multilevel Inverters

Levels/ Load	R load	RL load	RLC load	Motor load
9 level	14.49	14.58	14.48	14.51
11 level	12.82	12.95	12.80	12.82
13 level	10.43	10.54	10.22	10.44



CONCLUSION

This paper has discussed about the Selective Harmonic Elimination. The SHE method has been proposed and developed to reduce specific harmonics for multilevel inverters. Here, the odd numbers of switching angles are selected for reducing the lower order harmonics. The simulation result confirms that the lower order harmonics and THD has been effectively reduced to 10%. In this work, the lower order harmonics have been reduced by using the SHE method and by making use of the BEE Algorithm the switching angles are optimized to improve the output voltage quality but still it's found that the third order harmonics is with nominal magnitude of about 2 and the fifth and seventh order harmonics are further reduced by tuning the BEE algorithm. Therefore it's aimed to eliminate the LOH fully in future work.

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